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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/815,464 | 03/31/2004 | Todd B. Myers | 884.B60US1 | 6373 |

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

| EXAMINER | |
|---|---|
| PHAN, THIEM D | |
| ART UNIT | PAPER NUMBER |
| 3729 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 02/06/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/815,464 | MYERS ET AL. | |
| | Examiner | Art Unit | |
| | Tim Phan | 3729 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *32-37,39-45,69,70,72 and 73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-37,39-45,69,70,72,73* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 1/05/07 has been entered.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 32-37, 39-45 and 72 are rejected under 35 U.S.C. 102(e) as being anticipated by Schuster (US 20040113752).

**With regard to claim 32,** Schuster teaches a method of implementing electronic components in via-holes, comprising:

- forming a via (Fig. 2B, 3) in a substrate (Fig. 2, 2) through partial drilling, etching or punching or the like at one starting side of the substrate ;
- removing a portion of the via in the substrate to form a first via portion and a second via portion or additional portions further on the substrate to form a via-hole (Fig. 2B, 3); and
- forming an electrical component (Fig. 2E, 8) in the via in the substrate.

**With regard to claims 33 and 36,** Schuster teaches the forming at least of a portion of a resistor (Page 2, Section 0017).

**With regard to claims 34, 40 and 41,** Schuster teaches the forming at least of a portion of a capacitor or passive electrical component (Page 2, Section 0016).

**With regard to claims 35 and 37,** Crockett et al teach the forming at least of a portion of a core or magnetic actuator (Page 2, Section 0021).

**With regard to claim 39,** Schuster teaches the forming of a memory or piezoelectric element (Page 2, Section 0018).

**With regard to claims 42-44,** Schuster teaches the forming of an electrical component (Fig. 2E, 8) embedded in a via (Fig. 2E, 3).

The limitations of the claims "...a capacitor further comprising: ... an inner cylindrical portion (or a first curved portion) ... an outer via portion (or a second curved portion) ...." are

considered to be of a claimed article wherein the process for embedding an electric component in a via operates so this manner of operation does not distinguish over the process of Schuster, and Schuster at a minimum suggests the claimed method invention.

**With regard to claim 45,** Schuster teaches a method of implementing electronic components in via-holes, comprising:

- forming a via (Fig. 2B, 3) in a substrate (Fig. 2, 2); and
- forming at least of a portion of a transformer (Page 2, Section 0026) within the via.

**With regard to claim 72,** Schuster teaches a method of implementing electronic component in via-hole (Fig. 2E, 8; page 3, section 0082, lines 2-4), comprising the forming of a first electrical component from the first via portion and the forming of a second electrical component from the second via portion (Section 0082, lines 4-6) or resistor and capacitor in series.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 42 and 44 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Schuster in view of Figueroa et al (US 6,446,317).

**With regard to claim 42,** Schuster teaches a method of implementing electronic components in via-holes including a capacitor (Fig. 2E, 8; page 2, Section 0016), which reads on applicants' claimed invention; except for describing a capacitor structure.

Figueroa et al teach a method of fabricating a hybrid capacitor embedded in a via in order to get low inductance (Col. 3, lines 38-40), comprising:

- an inner cylindrical portion (Fig. 4, 406); and
- an outer via portion (Fig. 4, 404) substantially surrounding the inner cylindrical portion.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the detailed structure of the hybrid capacitor, as taught by Figueroa et al, to the method of embedding the capacitor in the via of Schuster in order to get low inductance in embedded circuitry.

**With regard to claim 44,** Schuster teaches a method of implementing electronic components in via-holes including a capacitor (Fig. 2E, 8; page 2, Section 0016), which reads on applicants' claimed invention; except for describing a capacitor structure.

Figueroa et al teach a method of fabricating a hybrid capacitor embedded in a via in order to get low inductance (Col. 3, lines 38-40), comprising:

- an inner cylindrical or first curved portion (Fig. 4, 406); and
- an outer via or second curved portion (Fig. 4, 404) substantially surrounding the inner

cylindrical portion or spaced from the first curved portion, wherein the first curved portion and the second curved portion are portions of a via formed by insulating (Fig. 4, 408) a first portion of a via from a second portion of a via.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the detailed structure of the hybrid capacitor, as taught by Figueroa et al, to the method of embedding the capacitor in the via of Schuster in order to get low inductance in embedded circuitry.

6. Claim 43 is further rejected under 35 U.S.C. 103(a) as being unpatentable over Schuster in view of Crockett et al (US 2002/0100612).

**With regard to claim 43,** Schuster teaches a method of implementing electronic components in via-holes including a capacitor (Fig. 2E, 8; page 2, Section 0016), which reads on applicants' claimed invention; except for describing a capacitor structure with a first curved portion and a second curved portion spaced from the first curved portion, wherein the distance between the first curved portion and the second curved portion varies.

Crockett et al teach a method for reducing the impedance within the reference within the printed circuit board including the forming of a capacitor (Fig. 2, 240) in the via in the substrate and the embedding of a capacitor of curvature shape (Figs. 3B & 3C, 240; page 3, section 0027, 2nd column, lines 1-9) in the via.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the curved structure of the capacitor, as taught by

Crocket et al, to the method of embedding the curved capacitor in the via of Crockett et al in order to have a variety of capacitors due to curved distance between portions or electrodes of the embedded capacitor, which in turn have varying dielectric thickness between portions or electrodes.

7. Claims 69 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crockett et al in view of Figueroa et al (US 6,446,317).

**With regard to claim 69,** Crockett et al teach a method for reducing the impedance within the reference within the printed circuit board, including the forming of a via (Fig. 2, 250B) in a substrate (Fig. 2, 200), the forming of a capacitor (Fig. 2, 240) in the via in the substrate and the embedding of a capacitor of different curvature shapes or inside/outside electrodes (Figs. 3B & 3C, 240) in the via, which read on applicants' claimed invention; except for having a varying distance between inside/outside portions or electrodes.

Figueroa et al teach a method of fabricating a hybrid capacitor embedded in a via, comprising:

- forming a first curved portion or inside electrode (Fig. 4, 406); and
- forming a second curved portion or outside electrode (Fig. 4, 404) spaced from the first curved portion by a dielectric (Fig. 4, 408), in order to increase levels of capacitance at reduced levels of inductance for decoupling, power dampening and supplying charge.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the method of fabricating the hybrid capacitor, as

taught by Figueroa et al, to the method of embedding the curved capacitor in the via of Crockett et al in order to increase levels of capacitance at reduced levels of inductance for decoupling, power dampening and supplying charge in a crowded circuitry while having a variety of capacitors due to curved distance between portions or electrodes of the embedded capacitor, which in turn have varying dielectric thickness or distance between portions or electrodes.

**With regard to claim 70,** Crockett et al teach a method for reducing the impedance within the reference within the printed circuit board, including the forming of a via (Fig. 2, 250B) in a substrate (Fig. 2, 200), the forming of a capacitor (Fig. 2, 240) in the via in the substrate and the embedding of a capacitor of curvature shapes or inside/outside electrodes (Figs. 3B & 3C, 240) in the via, which read on applicants' claimed invention; except for having insulation between the two portions or electrodes.

Figueroa et al teach a method of fabricating a hybrid capacitor embedded in a via, comprising:

- forming a first curved portion or inside electrode (Fig. 4, 406); and
- forming a second curved portion or outside electrode (Fig. 4, 404) spaced from the first curved portion by a dielectric (Fig. 4, 408), wherein the first portion and the second portion are portions of a via formed by insulating (Fig. 4, 408) a first portion or electrode of the via from a second portion or electrode of the via, in order to increase levels of capacitance at reduced levels of inductance for decoupling, power dampening and supplying charge.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the method of fabricating the hybrid capacitor, as taught by Figueroa et al, to the method of embedding the curved capacitor in the via of Crockett et al in order to increase levels of capacitance at reduced levels of inductance for decoupling, power dampening and supplying charge in a crowded circuitry while having a variety of capacitors due to curved distance between portions or electrodes of the embedded capacitor, which in turn have varying dielectric thickness or distance between portions or electrodes.

### *Allowable Subject Matter*

8. Claim 73 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Response to Arguments*

9. Applicants' arguments filed on 1/05/07 with respect to claims 32-37, 39-45, 69 and 70 have been considered but are moot in view of the new and current grounds of rejection.

## *Conclusion*

10. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M & Tu, 6AM - 2PM, and W & Th, 9AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tim Phan
Examiner
Art Unit 3729

tp
February 5, 2007